OPC Simplification and Mask Cost Reduction Using Regular Design Fabrics

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ABSTRACT

Cost and complexity associated with OPC and masks are rapidly increasing to the point that they could limit technology scaling in the future. This paper focuses on demonstrating the advantages of regular design fabrics for OPC simplification to enable scaling and minimize costs for technologies currently in volume production. The application of such a simplified OPC flow results in much smaller mask data volumes due to significantly fewer edges compared to the conventional designs and OPC flows. Moreover, the proposed approach enables reduced mask write times, hence lower mask costs.

We compare OPC performance and complexity on standard cell designs to that of layouts on a regular design fabric. We first demonstrate advantages and limitations within an industrial model-based OPC solution. Then, a simplified rule-based OPC solution is discussed for the Metal 1 layer. This simplified OPC solution demonstrates a 70X run time improvement and an order of magnitude reduction in both the output edge count per unit shape and shot count per unit shape while maintaining the printabalility advantages of regular design fabrics. The simplified OPC also demonstrates a 50% reduction in mask-write time. Finally, the benefit of regular design fabrics for OPC simplification and mask cost reduction at a 32nm node is discussed.

Keywords: Regular design fabrics, OPC, mask cost

1. INTRODUCTION

There has been a substantial increase in one time costs associated with the design and volume production of application specific integrated circuits ASICs [1]. An ASIC design start costs more than $10 Million [2]. Volume production of the ASIC requires a mask-set which costs close to $3 Million for 65nm technology node and in the range of $6 Million for the 32nm technology node (Figure 1). The increase in one-time costs disproportionately affects the manufacturing costs of low and medium volume products. It is no surprise that the industry has had fewer ASIC design-starts at sub-100nm process technologies [1, 3]. The charges incurred in purchasing a mask-set represent the bulk of the non-recurring costs per design for a lithography process [1]. The increase in mask costs is triggered with the use of complex OPC required to enable low k_1 optical lithography [3]. In this paper we discuss means of simplifying the complexity of OPC and reducing mask costs.

OPC is an integral part of all modern IC manufacturing flows. A simple concept based on correcting the mask design to compensate for inaccurate image transfer has evolved remarkably. What started as a simple rule-based OPC (RBOPC) strategy that applied corrections to the design based on the distance to the closest neighbor has evolved to the modern model-based OPC (MBOPC) that iteratively modifies the mask design to achieve optimum printability on silicon.

1.1. Growing Complexity Associated with Scaling in Low k_1 Regime

Decreasing pattern fidelity in the low k_1 regime has escalated the need for extensive modifications on the masks. Increased segmentation, more sophisticated use of sub resolution assist features (SRAFs) as well as layout decomposition for double patterning lithography are all required layout modifications to enable a sub-50nm process. OPC engines had to adapt to the requirements of these technologies. To make matters worse the wavelength of light used for optical lithography equipment has not been scaling. As the optical interaction range is dependent on the wavelength

of light used the optical interaction has stayed the same while feature dimensions and pitches are scaled at every subsequent process generation**.** This increases the number of layout shapes that must be considered by the OPC engines for every subsequent process generation.

Additionally the need to verify layout printability over the entire process window as well as a constant increase in the number of layers that require OPC has lead to a significant growth in the computational needs for OPC application [4]. Moreover, technologies such as "pixilated-phase masks" [5] and the need for "computational scaling" [6] further fuel the need for increasing computing resources for advanced process nodes. The introduction of server farms and hardware accelerated OPC has eased the computational challenge, but the growing cost and complexity of OPC is still paramount. It is anticipated that computational needs can rise to 100 CPU years [7] for modern process technologies.

1.2. Complex OPC Solutions for a Complex Design Space

The need for a supercomputer to render a mask design is mind boggling. If we had to print the same pattern repeatedly, using the same dimensions and same accuracy, the rendering of the mask pattern could be achieved even with a single CPU machines within minutes.

The complexity of the problem arises from the broad collection of different and unique layout patterns that are seen in varying product designs. The OPC algorithm is required to find a mask rendering that ensure adequate printability and yield, for all of the patterns that could possibly occur in the design. The only constraints on the design space are introduced by the layout design rules. For processes that see a large variety of designs with varying layout styles, an aggressive model-based OPC solution provides maximum flexibility to update and maintain the OPC algorithms that will ensure sufficient printability of rendered mask shapes over the broad spectrum of layout patterns. Model based OPC provides the additional advantage of being easily tunable with updated process simulation models.

1.3. Increasing Mask Cost

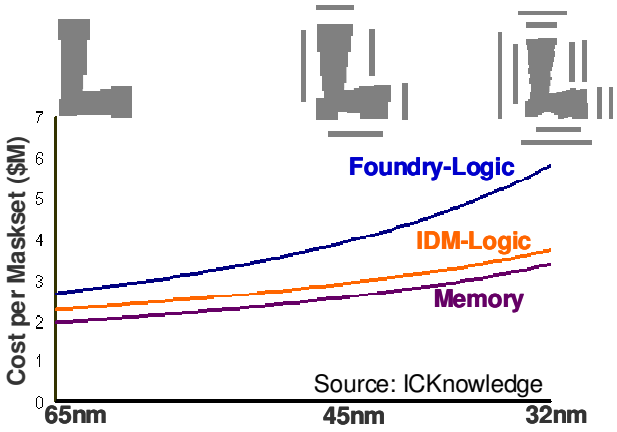


Figure 1: Increasing OPC complexity and mask costs

The application of model based OPC in conventional designs has not only increased the OPC costs by requiring additional computational resources and increased time to market, but it also lead to several challenges for mask manufacturing. Increased segmentation leads to a large number of edges, which results in increased shot counts for standard variable shape beam (VSB) tools. Although improvements in tool throughput have enabled mask shops to maintain a constant rate of productivity, it has been achieved at increasing cost. The cost of a toolset at 45nm has reached $80 million, up from $60 million for 90nm and it is anticipated to reach $100 million for the 22nm technology node [7]. This increase in tool cost is dominated by inspection tools that need to detect smaller defects in finer-segmented geometries. The challenges with both inspection and repair of the finer geometries introduced by model based OPC has lead to lowering mask yields along with increasing inspection and repair time [8]. The demand for tighter CD control is another contributor to increasing mask costs [9]. All along, the number of layers that require more complex OPC has been increasing at a factor of 2 for every generation [3], and the introduction of double patterning at 32nm technology and its widespread adoption for future processes has driven mask costs significantly higher. Figure 1 demonstrates the

increasing OPC complexity from the 65nm to the 32nm technology node and the corresponding increase in mask costs. Foundries that see a variety of designs with a spectrum of layout styles tend to implement and maintain a more aggressive OPC solution compared to integrated device manufacturers (IDM) and memory fabs. It is no surprise that foundries experience a more rapid increase in mask costs, as shown in Figure 1.

The only possible way to simplify the OPC solution is to simplify the problem itself. Layout simplification has been suggested for reducing OPC complexity; however prior to the use of regular design fabrics, it has not been proven in practice. In [10], Jhaveri et al. demonstrated the advantages of regular design fabrics for low cost production of ICs by extending the life of current generation lithography tools. In this paper we extend our previous work to demonstrate the advantages of regular design fabrics for simplifying OPC development and OPC application.

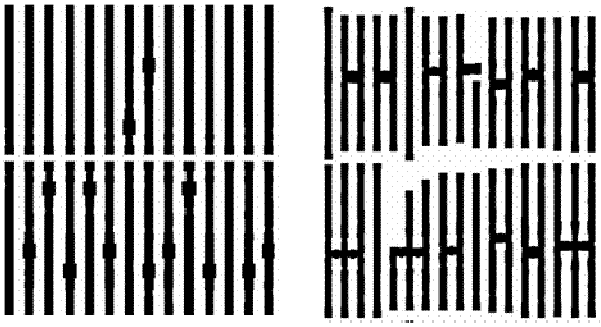
2. MODEL BASED OPC FOR SIMPLIFIED LAYOUTS

The desire for simplification, although noble, has not been achieved in practice until now. The ability to implement a design that consists of simplified layout patterns while achieving the same design performance specs of conventional standard cell designs is a significant contribution to current IC design and manufacturing technologies [11]. In our experiments we compare OPC on two design blocks: (a) a 65nm PowerPC 405 core and (b) a 65nm control block. Both designs have a standard cell implementation as well as an implementation employing regular design fabrics. The designs for the regular design fabrics is developed by PDF Solutions based on the pdBRIX technology and achieves the same power performance and area constraints as the standard cell design.

OPC runtimes, output segment counts per input shape and shot counts per input shape are compared between the original standard cell design and the extremely regular pdBRIX design. No change is made to the OPC algorithm. Shots count is computed by counting the total number of rectangles in the design. Where annotated with an (*) shot count is estimated as the upper bound to the number of rectangles.

2.1. Model-Based OPC for Poly Layer

We start our discussion with the poly layer. We only compare results on the PowerPC 405 design. Examples of the poly layer post OPC is shown in Figure 2. The pdBRIX design is unidirectional, with the only deviations from grating patterns occurring at the line-ends and poly landing pads. On the other hand, the poly layer in the standard cells is only regular at the gates. An illustration of layout irregularity at poly is shown in Figure 3b. One can notice that field poly (poly over isolation regions) constitutes of several arbitrary patterns.



(a) (b)

Figure 2: Poly layer model-based OPC (a) pdBRIX (b) Standard Cells

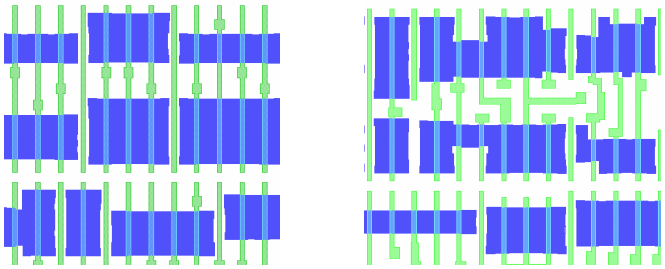
	Standard Cells	pdBRIX	Improvement by pdBRIX (%)
Total CPU time (sec)	552234	330361	43.40
Output edge per input shape	253.79	192.25	24.25
Assist features per input shape	0.39	0.08	79.80
Shot count per input shape	125.89*	95.124*	24.43

Table 1: Summary for poly layer with model-based OPC

Significant improvement in run-time and segment count is observed for extremely regular designs. As illustrated in Table 1, there is a 43.4% reduction in runtime, 24% lower output edges per unit input shape, 80% lower assist features per input shapes and a 24% reduction in shot count per input shape.

2.2. Model-Based OPC for Active Layer

Results for OPC complexity performed on the active layers of the PowerPC 405 are summarized in Table 2. There is a 66% reduction in runtime, a 16% reduction in output edge per unit input shape, a 16% reduction in shot count per unit input shape and most importantly, a total elimination of assist features per unit input shape with the use of regular patterning. It should be noted that the use of assist features requires smaller pixel size for inspection and as a results increases inspection time. The lack of assist features in the pdBRIX design will help reduce mask costs by reducing inspection time.



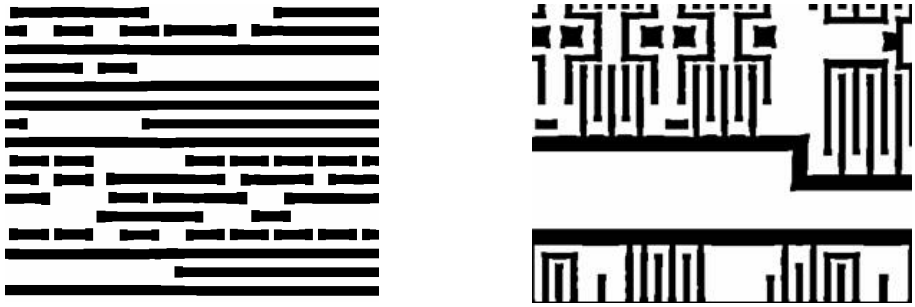
(a) **(b)**

Figure 3: Active layer model-based OPC (a) pdBRIX (b) Standard Cells

	Standard Cells	pdBRIX	Improvement by pdBRIX (%)
Total CPU time (sec)	**33653**	**11489**	**65.86**
Output edge per input shape	**76.56**	**64.32**	**15.99**
Assist features per input shape	**0.01**	**0.00**	**100.00**
Shot count per input shape	**37.28***	**31.25***	**16.42**

Table 2: Summary for active layer with model-based OPC

2.3. Model-Based OPC for Metal 1 Layer



(a) **(b)**

Figure 4: Metal layer model-based OPC (a) pdBRIX (b) Standard Cells

The study for Metal 1 (M1) is more elaborate. We compare OPC performance on both the PowerPC 405 and the control blocks. It is observed that the magnitude of improvement by the use of simplified layouts is strongly dependent on the design block. For the PowerPC 405 design that has a moderate M1 utilization (design density), a minimal improvement in OPC complexity is observed. Whereas, the control block that has extremely high M1 utilization demonstrates significant improvement for the pdBRIX design. Further, the results in Table 3 indicate that increasing design utilization decrease the number of edges per unit input shape as well as shot counts per unit input shape for pdBRIX but increases it

for the standard cell designs. The true reasons for these trends are inconclusive, but one can hypothesize that the grating like nature of the pdBRIX design benefits from the increased design density and requires fewer OPC corrections.

	Standard Cells		pdBRIX		Improvement by pdBRIX (%)	
	PPC405	Control Block	PPC405	Control Block	PPC405	Control Block
Total CPU time (sec)	226759	-	138124	-	39.09	-
Output edge per input shape	55.51	82.11	52.55	43.58	5.32	46.93
Shot count per input shape	26.75*	37.42	25.26*	14.48	5.57	61.30

Table 3: Summary for metal 1 layer with model-based OPC

3. SIMPLIFIED OPC FOR SIMPLIFIED LAYOUTS

The improvement in edge count and run time for an extremely regular design using model-based OPC is encouraging. However, the eventual goal of this research is not to provide an incremental improvement to current OPC techniques, but instead, to enable the simplification of modern OPC. We designed a simplified rule-based OPC for 65nm M1 layer. Our methodology differs from standard rule-based OPC for two distinct reasons: (a) dummy patterns are used to provide uniform density and (b) rule-based OPC is applied only to critical patterns, whereas the rest of the edges receive only a uniform biasing to avoid catastrophic failures.

	pdBRIX: MBOPC		pdBRIX: Simplified OPC		Improvement compared to standard cells (%)			
					MBOPC		Simplified OPC	
	PPC405	Control Block	PPC405	Control Block	PPC405	Control Block	PPC405	Control Block
Total CPU time (sec)	138124	NA	3201	-	39.09	-	98.59	-
Output edge per input shape	52.56	43.58	8.93	6.52	5.32	46.93	83.91	92.06
Shot count per input shape	25.26*	14.48	3.47*	1.63	5.57	61.30	85.47	95.64

Table 4: Summary for metal 1 layer with simplified rule-based OPC

The application of this simple rule-based OPC demonstrates a 98.6% reduction (70X reduction) in run-time as well as an order of magnitude reduction in both the output edge count per input shape as well as the shot count per input shape. The significant reduction in edge count enables reduction of mask costs by lowering mask-write times. Detailed discussion on mask-write time is left to Section 5.

4. PRINTABILITY ASSESSMENT

No OPC evaluation is complete without an analysis of printability. At 65nm, the simplified M1 layer in the pdBRIX design demonstrates significant advantage for OPC simplification. We now validate the printability of both standard cells and pdBRIX designs for the different OPC strategies discussed. Simulation under nominal process conditions shows adequate printability for pdBRIX layouts with both rule-based and model-based OPC. Standard cells on the other hand suffer from catastrophic failures with a simplified rule-based OPC. In order to successfully apply a rule-based solution to standard cell designs would require adding several more rules to the rule-based OPC solution. A more quantitative analysis of the printability results is summarized in Table 5.

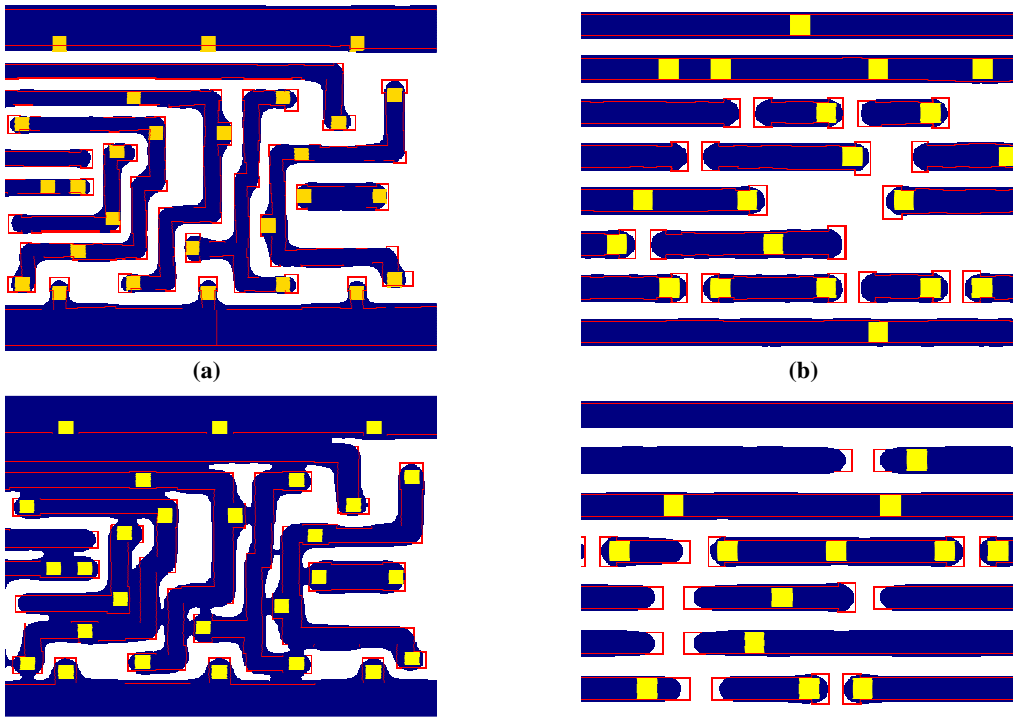


Figure 5: Nominal simulation on 65nm metal 1 (a) Standard cell with model-based OPC (b) pdBRIX with model-based OPC (c) Standard cell with rule-based OPC (d) pdBRIX with rule-based OPC

	Std cells Simple	Std cells MBOPC	pdBRIX Simple	pdBRIX MBOPC
Min Spacing	**X**	**72 nm**	**83 nm**	**84 nm**
Min Width	**X**	**97 nm**	**105nm**	**117 nm**
Min Coverage	**X**	**46%**	**78%**	**86%**

Table 5: Summary for printability assessment on metal 1 layer

A comparison of the two approaches on the pdBRIX design shows that a simplified OPC solution decreases the minimum width and minimum contact coverage (under worst case misalignment) compared to model-based solution. However, it is important to note that both the rule-based and model-based OPC solutions for the pdBRIX design demonstrate improved robustness to a model-based solution with a standard cell design. This is an encouraging result that allows us conclude that we can minimize OPC complexity, and do so without significantly lowering printability or impacting yield.

5. ANALYSIS OF MASK COSTS

Finally, to tie the improvement seen in OPC complexity to a more tangible metric we have estimated the mask-write times based on model proposed by Zhang [12]. The model predicts a linear fit for the total number of edges on the mask to the mask-write time. Results are summarized in Table 6. The notable conclusion from this analysis is that a 50% reduction is mask write time is observed by using simplified OPC for extremely regular designs.

		Standard Cells (min)	pdBRIX (min)		Improvement compared to Standard Cell (%)	
			model-based OPC	simplified OPC	model-based OPC	simplified OPC
PPC405	Poly	1072.71	589.00	-	45.09	-
	Active	276.48	186.03	-	32.72	-
	Contact	197.90	164.51	-	16.87	-
	Metal 1	349.92	227.45	166.39	35.00	52.45
Control Block	Metal 1	372.55	325.75	179.62	12.56	51.79

Table 6: Mask-write time estimates

As suggested, the NRE lithography costs are strongly influenced by OPC complexity**.** Increased OPC complexity has been accepted as it enables improved printability and yield. In doing so, we have extended the OPC development cycle, increased run-times as well as increased mask write times. Figure 6 summarizes the tradeoffs between mask cost and yield for products with varying volumes. Lithography costs per layer was determined based on model proposed by Menon et al [13] and lithography cost data reported by Lin [14]. A 5% improvement in yield reduces the lithography cost per layer by 5% over all product volume. In contrast, a 15% reduction in mask cost enables a cost reduction between 2.5%-10% depending on the product volume. The break-even cost occurs at a volume of 7500 wafers, where the benefit from a 5% yield improvement matches that of a 15% mask cost reduction. A strong argument can be made to define OPC and mask solutions based on product volumes. The benefits from reduced mask costs outweigh the improvement from yield for low and medium volume products. For high volume products the benefit from improving yields outweigh that from lowering mask costs.

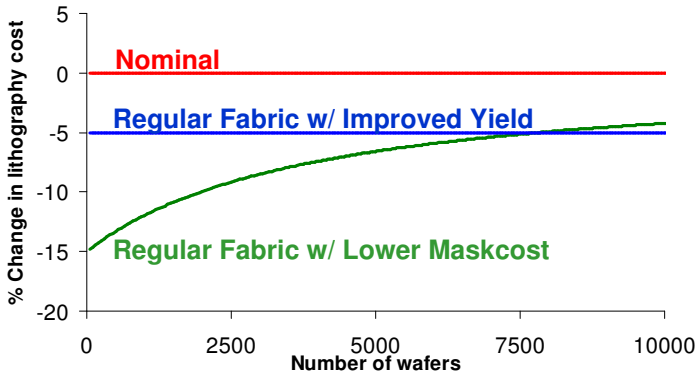


Figure 6: Implications on lithography cost per layer by improving yield or reducing mask costs as a function product volume

6. SIMPLIFIED MASKS FOR DOUBLE PATTERNING

The use of regular design fabrics not only helps lower mask costs for mature technologies but it can also enable economical scaling for future generations. The industry has adopted double patterning at the 32nm technology node. As a result, OPC engines must not only find a fairly complex OPC solution, but they must do so over two different mask designs. It is no surprise that computing resources required and the cost for mask-sets are rising dramatically. We demonstrate how simplified layouts can enable a lower cost solution by simplifying the OPC complexity and mask costs for double patterning. In this experiment we applied the same model-based OPC on two different 32nm layouts. In the post OPC design shown in Figure 7, the blue layer corresponds to the first patterning step, whereas the green corresponds to the second patterning step. The extremely regular pdBRIX design only requires very simple mask splitting and virtually no OPC, whereas the standard cell layout requires fairly aggressive OPC for both mask layers, thus demonstrating a simpler RET and OPC solution for simplified layouts.

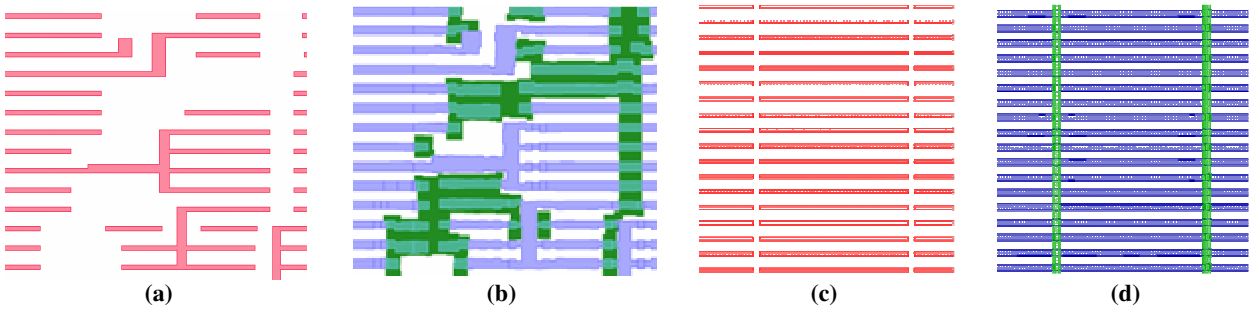


Figure 7: 32nm Poly (a) Standard cell design (b) Standard Cell OPC (c) pdBRIX design (d) pdBRIX OPC

CONLUSIONS

This paper illustrates how simplifying design style can enable simplified OPC flows that reduce OPC runtimes as well as output edge counts. This reduced edge count can significantly reduce mask costs and will enable more design starts for the sub-50nm process technologies. The highlight of the paper is the demonstration of a simplified rule-based OPC that can reduce OPC run times by 70X as well as reduce output edge count per input shape and shout count per input shape by an order of magnitude, as compared to model-based OPC on standard cell designs without degrading printability significantly. This improvement in OPC complexity also leads to a 50% reduction in mask-write times. We further described the advantages of extremely regular designs to simplify OPC and mask manufacturing for double patterning lithography.

ACKNOWLWDGEMENTS

The authors would like to acknowledge the design teams at IBM and PDF Solutions for providing the designs of the PowerPC 405 and the control block. The authors would also like to thank Marcin Strojwas at PDF Solutions for the discussions on industry trends and forecasts.

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